

United States Patent and Trademark Office



UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,740	01/24/2002	Hong Guo	03745.0009	4249
22852	7590 07/13/2005		EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER			VO, LILIAN	
LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			ART UNIT	PAPER NUMBER
			2195	
			DATE MAILED: 07/13/200	5

Please find below and/or attached an Office communication concerning this application or proceeding.

		·				
	Application No.	Applicant(s)				
Office Action Summers	10/053,740	GUO ET AL.				
Office Action Summary	Examiner	Art Unit				
	Lilian Vo	2195				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 24 January 2002.						
2a) ☐ This action is FINAL . 2b) ☑ This action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the ments is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
 4) Claim(s) 1 - 21 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) is/are allowed. 6) Claim(s) 1 - 21 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement. 						
Application Papers						
9)☐ The specification is objected to by the Examiner. 10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.						
	Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
		,				
Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)						
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	5) Notice of Informal F 6) Other:	atent Application (PTO-152)				
J.S. Patent and Trademark Office						

Art Unit: 2195

DETAILED ACTION

1. Claims 1-21 are pending.

Claim Objections

2. Claims 2 and 6 are objected to because the examiner believes there is a typographical error, an extra comma after the word "and". Appropriate correction is required.

Claim Rejections - 35 USC § 112

- 3. Claims 1-9, 12, 14-16 and 20-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 4. Claims 3, 5, 12, 20, 21 recite the limitation a required radius is considered unclear. A radius required was not mention anywhere in the preceding claims. How is required radius related to executing the job? For the purpose of the examination, the examiner will assume it referring to allocate the jobs to the one group of node boards on the basis of which group of node boards have CPUs available to execute jobs for each radius. A clarification is required.
- 5. Claim 6 recites the limitation "a job execution unit for receiving jobs which have been scheduled to the selected host by the job scheduling unit" is considered unclear. Does that mean a job execution unit receives jobs that have been scheduled by itself? Clarification is required.

Page 3

Application/Control Number: 10/053,740

Art Unit: 2195

- 6. The following terms lack of antecedent basis:
 - a. "the central processing units", in claims 1, 4 and 9.
 - b. "the jobs", in claims 1, 3 and 6.
 - c. "said batch scheduling system", in claims 1 and 4 9.
 - d. "the scheduler", in claim 7.
 - e. "the selected", in claim 7.
 - f. "the access", in claim 9.
 - g. "the expected", in claim 14.
 - h. "the group", in claims 14, 15 and 16.
 - i. "the job", in claims 15, 20 and 21.
 - j. "the number", in claim 16.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

- 8. Claims 10 12 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.
- 9. Claims 10 12 are directed to method steps, which can be practiced mentally in conjunction with pen and paper, therefore they are directed to non-statutory subject matter.
 Specifically, as claimed, it is uncertain what performs each of the claimed method steps.

Application/Control Number: 10/053,740

Art Unit: 2195

Moreover, each of the claimed steps, inter alias, <u>assessing</u>, <u>comparing</u>, <u>scheduling</u>, can be practiced mentally in conjunctions with pen and paper. The claimed steps do not define a machine or computer implemented process [see MPEP 2106]. Therefore, the claimed invention

is directed to non-statutory subject matter. (The examiner suggests applicant to change

"method" to "computer implemented method" in the preamble to overcome the outstanding 35

U.S.C. 101 rejection).

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 11. Claims 1, 2 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimmel et al. (US. 6,105,053, hereinafter Kimmel).
- Regarding claim 1, Kimmel discloses a computer system comprising a cluster of node boards, each node board having least one central processor unit (CPU) and shared memory, said node boards being interconnected into groups of node boards providing access between the central processing units (CPUs) and shared memory on different node boards, a scheduling system to schedule a job said node boards which have resources to execute the jobs, said batch scheduling system (abstract) comprising:

topology monitoring unit for monitoring a status CPUs and generating status information signals indicative of the status of each group of node boards (abstract, col. 2, lines 19-21:

Art Unit: 2195

means for monitoring the activity of the processors and selecting processes queued in the run queues for the processors to execute. Col. 2, lines 36 – 46: a dispatcher associated with each processor for monitoring a run queue of the associated processor, which looks for and obtains processes from the run queues of the other processors to execute);

job scheduling unit for receiving said status information signals and said jobs, and scheduling the job to one group of node boards on the basis of which group of node boards have the resources required execute the job as indicated by the status information signals (col. 2, lines 22 - 35, 46 - 57).

- Regarding claim 2, Kimmel discloses the scheduling system defined in claim 1 wherein the status information signals indicate which CPUs in each group of node boards have available resources, and, the job scheduling unit schedules jobs to groups of node boards which have resources required to execute the job (col. 2, lines 19 35, 46 57, col. 13, lines 4 30).
- 14. Claim 13 is rejected on the same ground as stated in claim 1 above.

Claim Rejections - 35 USC § 103

- 15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Art Unit: 2195

16. Claims 3, 4, 14 – 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al. (US. 6,105,053).

- 17. Regarding **claim 3**, Kimmel discloses the status information signals for each group of node boards indicate the CPUs available to execute jobs (col. 2, lines 19 21), and wherein the job scheduling unit allocates the job to the one group of node boards on the basis of which group of node boards have CPUs available to execute jobs (col. 8, lines 39 44). Kimmel further discloses that his system provides a global scheduling mechanism for maintaining a balanced processor load across the system while increasing system throughput (col. 2, lines 22 32, col. 10, lines 34 49). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to recognize that Kimmel maintaining balanced processor load across the system must considered the availability of the resources before allocating the job to a particular resource.
- Regarding claim 4, Kimmel discloses the cluster of node boards are located on separate hosts (fig. 1B); and wherein the topology monitoring unit monitors the status of the CPUs in each host and generates status information signals regarding groups of node boards each host (col. 5, lines 42 57).
- 19. Regarding claim 14, Kimmel discloses the job scheduling unit schedules the jobs based on predetermined criteria (col. 13, lines 22 31). Kimmel discloses that trips to higher level shared memory to get data not located in the caches introduce delay into the processing of the thread and impact overall system throughput and that accessing far memory also introduce

Art Unit: 2195

delays (col. 8, lines 56 - 60, col. 11, lines 52 - 61). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to recognize that the expected delay to transfer information amongst the group of processors based on the physical topology and the status information signals have been considered as a criteria in Kimmel's scheduling system.

- 20. Regarding claim 15, Kimmel discloses the predetermined criteria include a radius of the group of processors to execute the job (col. 8, lines 56 60, col. 11, lines 52 61).
- 21. Regarding **claim 16**, Kimmel discloses the predetermined criteria further include the number of connections in the physical topology within the group processors, availability of memory associated with the group of processors and availability of other processors connected to the group of processors (figs. 1A, 1B, col. 4, lines 18 65, col. 8, lines 56 60, col. 11, lines 52 61).
- Regarding claim 17, Kimmel discloses the plurality of processors are physically located in separate modules (fig. 1B), wherein the topology monitoring unit comprises topology daemons associated with each module for monitoring a status of the processors physically located in the associated module and generating module status information signals indicative of the status of the processors in the associated module (col. 2, lines 22 35, 46 57), wherein the job scheduling unit receives the module status information signals from all of the topology daemons and allocates the jobs to a group of processors in one of the modules on the basis of the physical topology of the processors in the modules and the module status information signals from all of the modules (col. 2, lines 19 35, 46 57, col. 13, lines 4 30).

Art Unit: 2195

- 23. Regarding claim 20, Kimmel discloses the status information signals for each group of node boards indicate the CPUs available to execute jobs (col. 2, lines 19 21), and wherein the job scheduling unit allocates the job to the one group of node boards on the basis of which group of node boards have CPUs available to execute jobs (col. 8, lines 39 44). Kimmel further discloses that his system provides a global scheduling mechanism for maintaining a balanced processor load across the system while increasing system throughput (col. 2, lines 22 32, col. 10, lines 34 49). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to recognize that Kimmel maintaining balanced processor load across the system must considered the availability of the resources before allocating the job to a particular resource.
- 24. Claims 5 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al. (US. 6,105,053), as applied to claim 1 above, in view of Bitar et al. (US 6,353,844, hereinafter Bitar).
- Regarding claim 5, Kimmel discloses the status information signals include, for each host, a number of CPUs, which are available for each radius (col. 2, lines 1 9 21, col. 5, lines 42 57). Kimmel did not clearly disclose the scheduling unit maps the job to a selected host having a maximum number of CPUs available. Nevertheless, Bitar disclose a batch scheduler, which allocates resource based on the available resources (col. 2, lines 47 48, col. 4, lines 57 65, col. 7, lines 53 59). Therefore, it would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate the concept in Bitar's together with

Application/Control Number: 10/053,740

Art Unit: 2195

Kimmel to schedule the job with the most available resource so that job execution can be completed by its deadline.

Regarding claim 6, Kimmel discloses for each host, job execution unit for receiving jobs which have been scheduled to the selected host by the job scheduling unit, and, allocating the jobs to the selected group of node boards (col. 2, lines 36-46); and

wherein the job execution unit communicates with the topology monitoring unit allocate the jobs to the group node boards which the topology monitoring unit has determined have the resources required to execute the job (col. 2, lines 36- 46, col. 5, lines 42 - 50).

- 27. Regarding claim 7, Kimmel discloses the scheduler comprises a standard scheduler for allocating jobs to the selected group of node boards (col. 2, lines 36 57: medium scheduler) and an external scheduler for receiving the status information signals from the topology monitoring unit and selecting the selected group of node boards based on the status of the information signals (col. 2, lines 19 41).
- Regarding claim 8, Kimmel discloses if the job scheduling unit cannot locate a group of node boards which have the resources required execute the job scheduling unit delays allocation of the job until the status information signals indicate the resources required execute the job are available (col. 8, lines 39 44).

Art Unit: 2195

Regarding claim 9, Kimmel discloses the access between the central processing units (CPUs) and shared memory on different node boards is non-uniform (fig. 1A and 1B, col. 4, lines 18-65).

30. Regarding claim 10, Kimmel discloses a computer system comprising resources physically located in more than one module, said resources including a plurality of processors being interconnected by a number of interconnections physical topology providing non-uniform access to other resources said computer system (fig. 1A and 1B, col. 4, lines 18 – 65), a method of scheduling a job to said resources, said method comprising the steps of:

periodically assessing a status the resources and sending status information signals indicative of the status of the resources to a job scheduling unit (col. 2, lines 19 - 57); and

scheduling the job to the resources, which are available to execute the job as, based on the status information signals and the physical topology, and the resources required execute the job (col. 2, lines 36-46, col. 5, lines 42 - 50).

Kimmel did not clearly disclose the step of assessing, at the job scheduling unit, the resources required to execute job and comparing the resources required to execute the job and resources available based on the status information signals. Nevertheless, Bitar discloses the steps of assessing at the job scheduling unit the resources requires to execute the job (col. 4, lines 35-41) and comparing the resources required to execute the job and resources available based on the status information signals (col. 6, lines 9-20, 63-65, col. 7, lines 25-31, 53-59). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to combine the concept from Bitar's with Kimmel to schedule the job according to the available resources so that job execution can be completed by its deadline.

Art Unit: 2195

31. Regarding claim 11, Kimmel discloses the sub-step of:

periodically assessing the status of resources each module and sending status information signals indicative of the status of the resources in each module to the job scheduling unit (col. 2, lines 19 - 57).

Kimmel did not clearly discloses the step of comparing the available resources in each module the resources required to execute the job, and scheduling the job to module having the most resources available to execute the job. Nevertheless, Bitar discloses the steps of comparing the resources required to execute the job and resources available based on the status information signals (col. 6, lines 9 - 20, 63 - 65, col. 7, lines 25 - 31, 53 - 59), and scheduling the job that based on the available resources (col. 2, lines 47 - 48, col. 4, lines 57 - 65, col. 7, lines 53 - 59). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to combine the concept from Bitar's with Kimmel to schedule the job according to the available resources so that job execution can be completed by its deadline.

32. Regarding claim 12, Kimmel discloses the sub-steps

for each module, periodically assessing status of the resources by assessing the status of each processor in each module and sending to the job scheduling unit module status information for each module indicative of a number available processors at each radius in the module (col. 2, lines 19 - 57).

Kimmel did not clearly disclose the additional limitation as claimed. Nevertheless, Bitar discloses the steps of assessing, at the job scheduling unit, the requirements necessary to execute the job by determining the number processors required to execute the job (col. 4, lines 35 – 41),

Art Unit: 2195

comparing the resources required to execute the job and the resources available by comparing the number of processors required to execute the job and the number of available processors based on the module information status signals (col. 6, lines 9 - 20, 63 - 65, col. 7, lines 25 - 31, 53 - 59), and scheduling the job to the module which has a largest number of available processors the required radius based on the module status information signals and the physical topology (col. 2, lines 47 - 48, col. 4, lines 57 - 65, col. 7, lines 53 - 59). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to combine the concept from Bitar's with Kimmel to schedule the job according to the available resources so that job execution can be completed by its deadline.

- 33. Claims 18 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al. (US. 6,105,053), as applied to claim 13 above, in view of Thorson et al. (US 6,643,764, hereinafter Thorson).
- Regarding **claim 18**, Kimmel did not clearly disclose the additional limitation as claimed. Nevertheless, Thorson discloses the modules are interconnected by a META router operating on network (col. 4, lines 40 62, col. 5, lines 10 27), wherein the jobs and the module status information signals are communicated through the META router and network (col. 4, lines 40 62). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate Thorson's teaching with Kimmel's system to utilize an improved infrastructure.

Art Unit: 2195

Regarding claim 19, modified Kimmel discloses the system operating on a network (col. 4, lines 40 - 62) but did not clearly disclose the network comprise an internet. Nevertheless, the internet network is considered well known in art. It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to implement modified Kimmel's system with an internet to provide communication between the processing nodes.

- Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al. (US. 6,105,053) in view of Thorson et al. (US 6,643,764, hereinafter Thorson), as applied to claim 13 above, and further in view of Bitar et al. (6,353,844).
- 37. Regarding **claim 21**, modified Kimmel did not clearly disclose the step of scheduling the job to module having the most resources available to execute the job. Nevertheless, Bitar discloses the step scheduling the job that based on the available resources (col. 2, lines 47 48, col. 4, lines 57 65, col. 7, lines 53 59). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to combine the concept from Bitar's to modified Kimmel to schedule the job according to the available resources so that job execution can be completed by its deadline.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Friday, 8am - 4:30pm.

Art Unit: 2195

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist at 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo Examiner Art Unit 2195

lv July 8, 2005

ISORY PATENT EXAMINER